Intel® 830 Chipset Family

Design Guide Update

February 2005

Notice: The 830 chipset may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

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Contents

Revision History

Version	Description	Date
001	Initial Release	July 2002
002	Added Schematic, Layout, and Routing Updates #1	February, 2005

Preface

This document is an update to the design guidelines contained in the documents listed in the following Affected Documents table. It is a compilation of document changes, and is intended for hardware system manufacturers.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

Affected Documents

Document Title	Document Number
Intel® 830 Chipset Platform Design Guide January 2002	298339-003

Nomenclature

General Design Considerations include system level considerations that the system designer should account for when developing hardware or software products using the Intel® 830 Chipset.

Schematic, Layout, and Routing Updates include suggested changes to the current published schematics or layout, including typos, errors, or omissions from the current published documents.

Documentation Changes include suggested changes to the current published design guide not including the above.

Codes Used in Summary Table

Doc	Document change or update that will be implemented.
Shaded	This item is either new or modified from the previous version of the document.

NO.	Plans	General Design Considerations
		There are no General Design Considerations for this Design Guide Update

NO.	Plans	Schematic, Layout, and Routing Updates
1	Doc	Correction on IMVP-II connection

NO.	Plans	Documentation Changes
		There are no Documentation Changes for this Design Guide Update

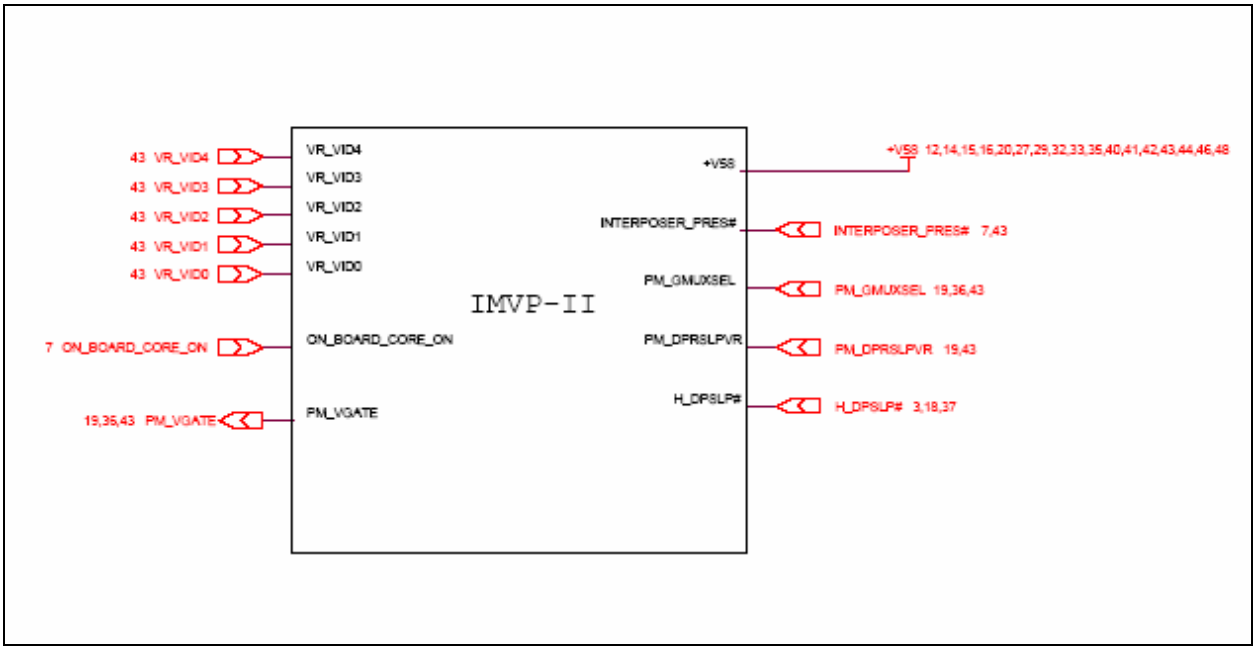
General Design Considerations

There are no General Design Considerations for this Design Guide Update.

Schematic, Layout, and Routing Updates

1. Correction on IMVP-II connection

Schematics net connections for IMVP-II should be corrected as follows (schematics sheet 45).



Documentation Changes

1. GMBus pullup recommendation

The following replaces section 6.5 of the design guide

The Intel® 830M/830MG Chipset GMCH-M DVOA, DVOB and DVOC ports control the video front-end devices via the GMBUS (I2C) interface. The Intel 830M/830MG Chipset GMCH-M has 5 GMBUS pairs that can be used in any combination of DVO ports (DVOA, DVOB or DVOC). The protocol and bus are used to configure registers in the TV encoder, TMDS/LVDS transmitter chips and the Intel® VCH chip. The GMCH-M also has an option to utilize the DDC2CLK and DDC2DATA to collect EDID (Extended Display Identification) from a digital display panel.

The GMBUS should be connected to the DVO device, as required by the specifications for those devices. DDC1_DATA and DDC1_CLK should be connected to the CRT connector. DDC2_DATA and DDC2_CLK should be connected to the DVI connector, as specified by the DVI specification. Typically 4.7 kΩ – 10 kΩ pull-ups (or pull-ups with the appropriate value derived from simulating the signal) are required on each of these signals**. When using a 10kΩ pull-up on the GMBus, some systems may exhibit loss of panel display or display artifacts. Trace routing, board stack-up and system noise may cause false clocking, resulting in register read/write errors. A stronger pull-up, such as 4.7kΩ, is recommended for system implementations susceptible to noise or long rise times on the GMBus**.

The following 830M/MG GMCH-M signal groups list the five possible GMBUS pairs.

- DDC1_CLK / DDC1_DATA
- I2C_CLK / I2C_DATA
- DDC2_CLK / DDC2_DATA
- M_I2C_CLK (G_IRDY#) / M_I2C_DATA (G_DEVSEL#)
- M_DDC1_CLK (G_TRDY#) / M_DDC1_DATA (G_FRAME#)

If any of the five GMBUS pairs signals are not used; 4.7K – 100 KΩ pull-up (or pull-ups with the appropriate value derived from simulating the signal) resistors are required. This will prevent the GMCH-M DVOA interface from confusing noise on these lines for false cycles.

If muxed DVOs are being used, please note that G_PAR should be pulled down to ground on the platform using a 330-Ohm resistor.

2. TFLT_MAX and TFLT_Min Calculation Update

Updates to section 3.2.1 of the design guide. Replaces Table 2 and Table 3 and their component definitions with the following (Tp-p and Madj removed):

Table 2 and Table 3 are derived using the following timing components:

- Clk_{SKEW}= The maximum allowable skew between the 133-MHz clocks driven by the clock chip to the processor and GMCH-M **and includes pin-to-pin skew and trace length mismatches on clk nets. Assumed to be 250 ps.**
    - Clk_{JITTER}= The maximum allowable short-term variation in the clock edge from its ideal position Assumed to be 200 ps.

See the respective processor datasheet and appropriate Intel® 830 Chipset family documentation for details on clock skew and jitter specifications. Exact details of host clock routing topology are provided with the platform design guideline.

Table 2. Example TFLT_MAX Calculations for 133-MHz Bus

Driver	Receiver	T_{CYC}	T_{CO_MAX}	T_{SU_MIN}	Clk_{SKEW}	Clk_{JITTER}	Recommended T_{FLT_MAX}
Processor	GMCH-M	7.50	3.25	2.65	0.25	0.20	1.15
GMCH-M	Processor	7.50	4.10	0.95	0.25	0.20	2.00

Note: $T_{FLT\_MAX} = T_{CYC} – T_{CO\_MAX} – T_{SU\_MIN} – Clk_{SKEW} - Clk_{JITTER}$

Table 3. Example FLT_MIN Calculations (Frequency Independent)

Driver	Receiver	T_{HOLD}	T_{CO_MIN}	Clk_{SKEW}	Recommended T_{FLT_MIN}
Processor	GMCH-M	7.50	3.25	0.25	1.15
GMCH-M	Processor	7.50	4.10	0.25	2.00

Note: $T_{FLT\_MIN} = T_{HOLD} – T_{CO\_MIN} + Clk_{SKEW}$

3. PSB address, data, control routing guidelines update

Updates to section 3.3 of the design guide. Replaces Table 4, Table 5 and Table 6 with the following:

Table 4. Processor System Bus Data Signal Routing Guidelines

Signal Names		Topology	Total Trace Length		Nominal Impedance (ohms)	Width and Spacing (mils)
CPU	GMCH-M		Max (inches)	Min (inches)		
D[63:0]#	HD[63:0]#	TOP 1	4	1.1	55 ± 15%	5 & 10

Table 5. Processor System Bus Address Signal Routing Guidelines

Signal Names		Topology	Total Trace Length		Nominal Impedance (ohms)	Width and Spacing (mils)
CPU	GMCH-M		Max (inches)	Min (inches)		
A[31:3]#	HA[31:3]#	TOP 1	4	1.1	55 ± 15%	5 & 10

Table 6. Processor System Bus Control Signal Routing Guidelines

Signal Names		Topology	Total Trace Length		Nominal Impedance (ohms)	Width and Spacing (mils)
CPU	GMCH-M		Max (inches)	Min (inches)		
RESET#	CPURST#	TOP 2	4	1.1	55 ± 15%	5 & 10
BNR#	BNR#	TOP 1	4	1.1	55 ± 15%	5 & 10
REQ[4:0]#	HREQ[4:0]#	TOP 1	4	1.1	55 ± 15%	5 & 10
BPRI#	BPRI#	TOP 1	4	1.1	55 ± 15%	5 & 10
DEFER#	DEFER#	TOP 1	4	1.1	55 ± 15%	5 & 10
LOCK#	HLOCK#	TOP 1	4	1.1	55 ± 15%	5 & 10
TRDY#	HTRDY#	TOP 1	4	1.1	55 ± 15%	5 & 10
DRDY#	DRDY#	TOP 1	4	1.1	55 ± 15%	5 & 10
ADS#	ADS#	TOP 1	4	1.1	55 ± 15%	5 & 10
DBSY#	DBSY#	TOP 1	4	1.1	55 ± 15%	5 & 10
HIT#	HIT#	TOP 1	4	1.1	55 ± 15%	5 & 10
HITM#	HITM#	TOP 1	4	1.1	55 ± 15%	5 & 10
RS[2:0]#	RS[2:0]#	TOP 1	4	1.1	55 ± 15%	5 & 10
NOTE:	Trace width of 5 mils and trace spacing of 10 mils within signal groups.					
	Spacing between signal groups (address, data and control) should be 25 mils and					
	other (3.3 V) signals should be 25 mils					